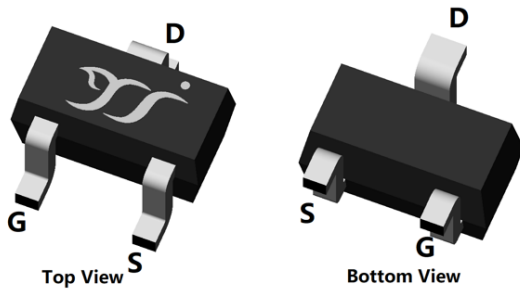
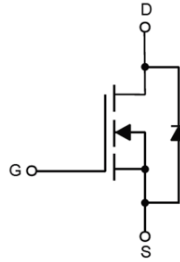


## N-Channel Enhancement Mode Field Effect Transistor



**SOT-523**



### Product Summary

- $V_{DS}$  60V
- $I_D$  0.3A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ )  $< 1.4\Omega$
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ )  $< 1.6\Omega$

### General Description

- Trench Power MV MOSFET technology
- Voltage controlled small signal switch
- Low input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- Battery operated systems
- Solid-state relays
- Direct logic-level interface: TTL/CMOS

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	60	V
Gate-source Voltage	$V_{GS}$	$\pm 30$	V
Drain Current	$I_D$	$T_A=25^\circ C$	0.3
		$T_A=100^\circ C$	0.19
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	1.5	A
Total Power Dissipation <sup>B</sup>	$P_D$	$T_A=25^\circ C$	0.3
		$T_A=100^\circ C$	0.1
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ C$

### ■ Thermal resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>C</sup>	$R_{\theta JA}$	350	420	$^\circ C/W$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
2N7002E	F2	7002.	3000	30000	120000	7" reel



# 2N7002E

RECOMMEND  
2N7002BE  
FOR NEW DESIGN

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	μA
		V <sub>DS</sub> =60V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	-	-	100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±30V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.6	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =0.3A	-	1.0	1.4	Ω
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =0.2A	-	1.15	1.6	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =0.3A, V <sub>GS</sub> =0V	-	0.85	1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz	-	6.5	-	Ω
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	0.3	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>		-	36	-	pF
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, f=1MHz	-	5.2	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	2.2	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>		-	1.6	-	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =0.3A	-	0.47	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	0.25	-	
Reverse Recovery Charge	Q <sub>rr</sub>		-	2.5	-	nC
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> =0.3A, di/dt=100A/us	-	11.5	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>		-	3.3	-	ns
Turn-on Rise Time	t <sub>r</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =30V, I <sub>D</sub> =0.3A R <sub>GEN</sub> =6Ω	-	19	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	9.6	-	
Turn-off fall Time	t <sub>f</sub>		-	49	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. P<sub>d</sub> is based on max. junction temperature, using junction-case thermal resistance.

C. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in the still air environment with T<sub>A</sub> =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

## Typical Electrical and Thermal Characteristics Diagrams

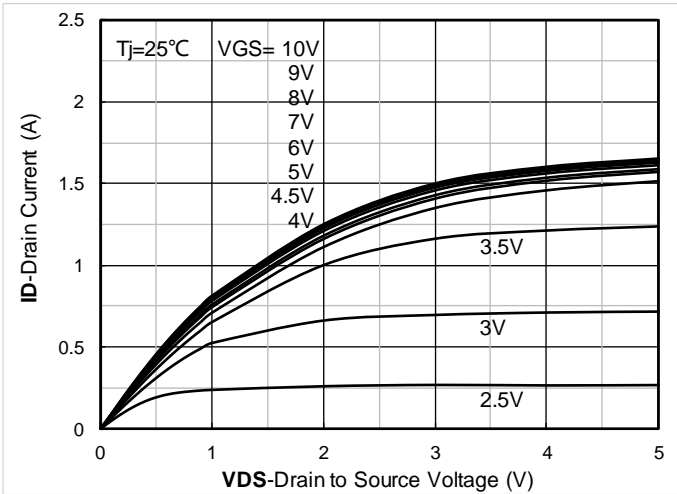


Figure 1. Output Characteristics

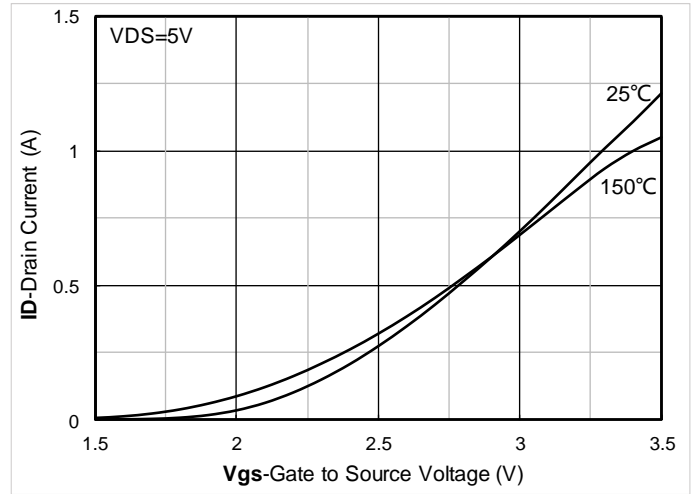


Figure 2. Transfer Characteristics

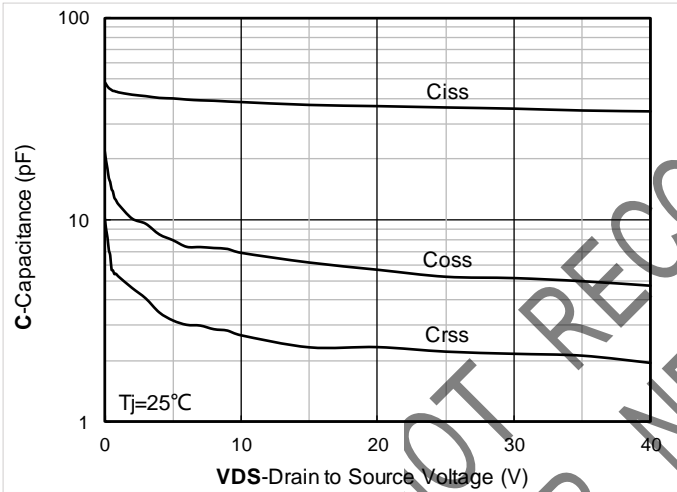


Figure 3. Capacitance Characteristics

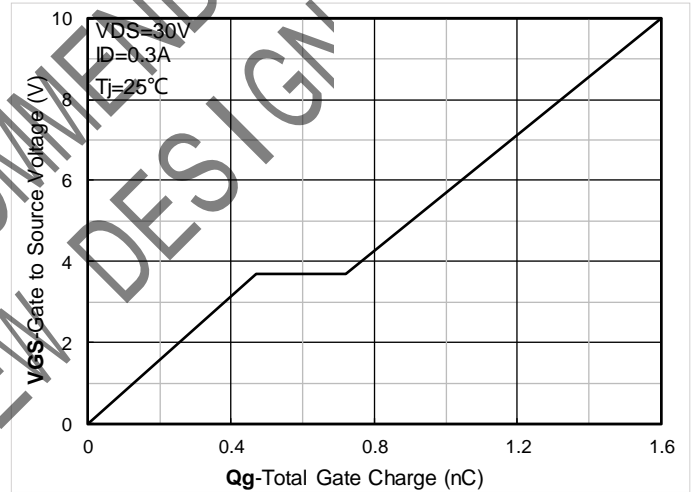


Figure 4. Gate Charge

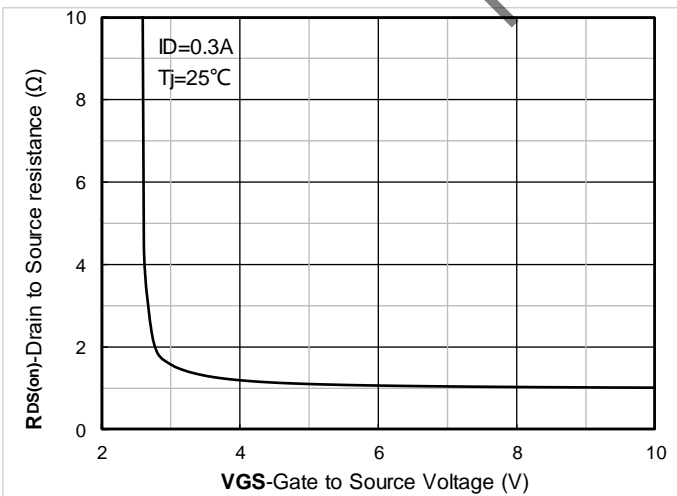


Figure 5. On-Resistance vs Gate to Source Voltage

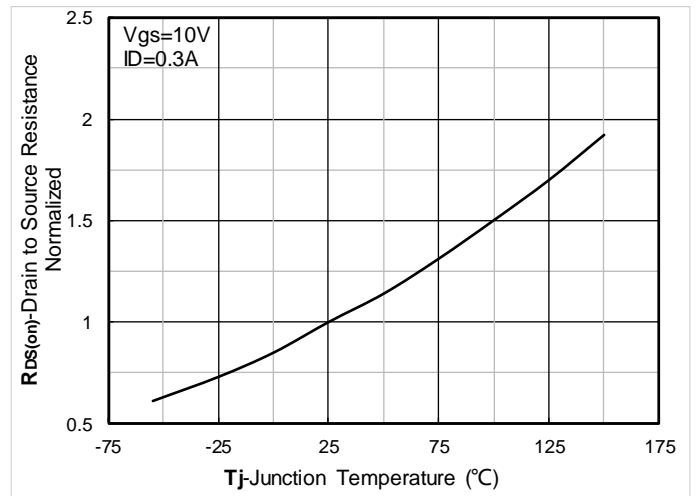


Figure 6. Normalized On-Resistance

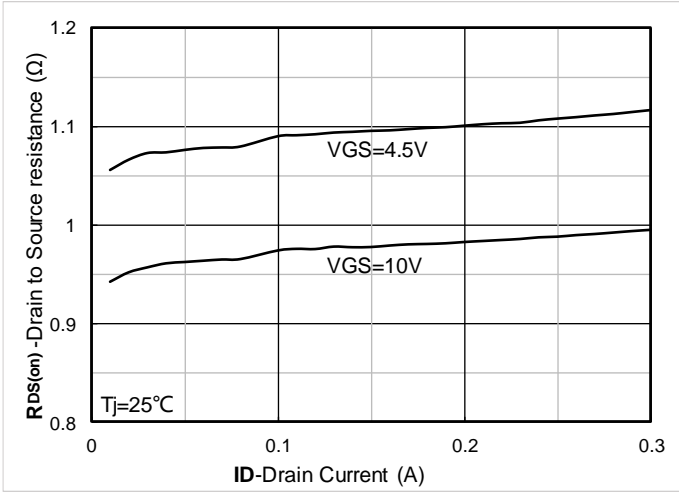


Figure 7.  $R_{DS(on)}$  VS Drain Current

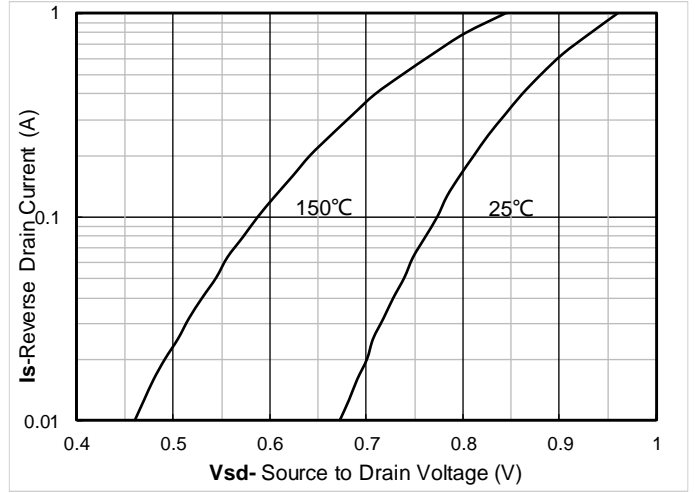


Figure 8. Forward characteristics of reverse diode

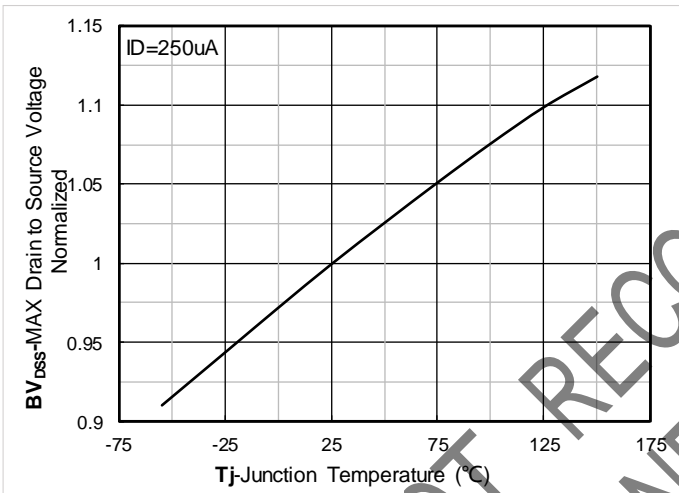


Figure 9. Normalized breakdown voltage

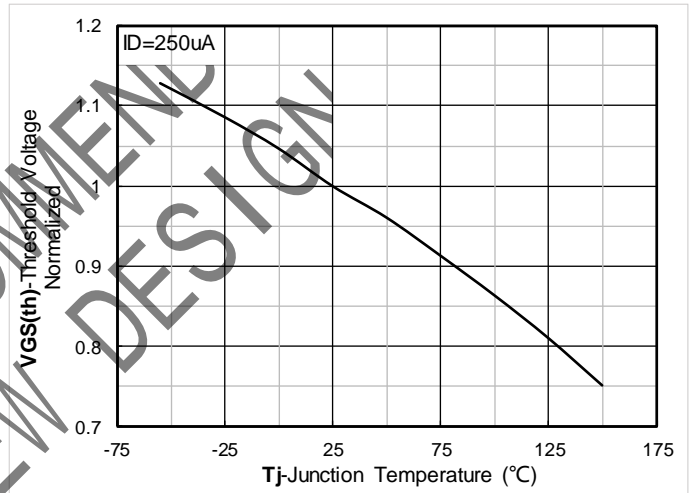


Figure 10. Normalized Threshold voltage

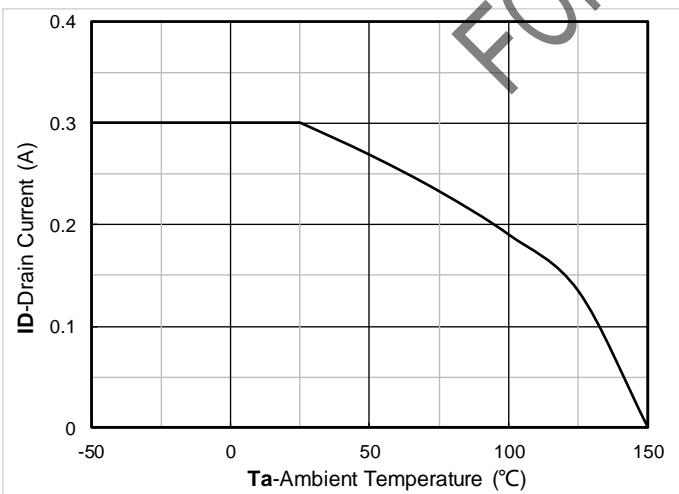


Figure 11. Current dissipation

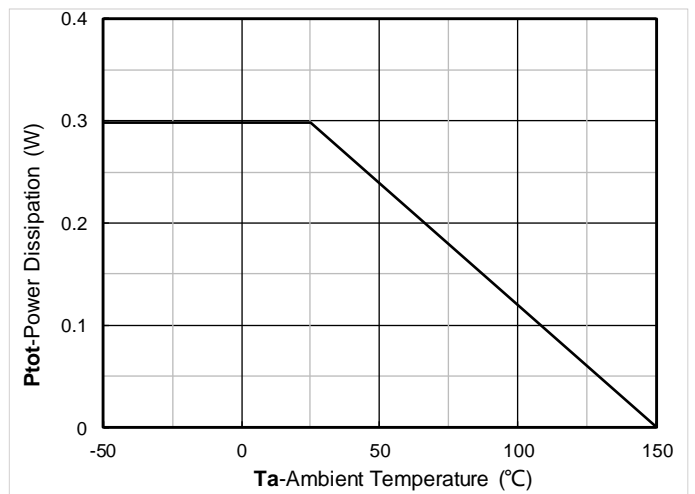


Figure 12. Power dissipation

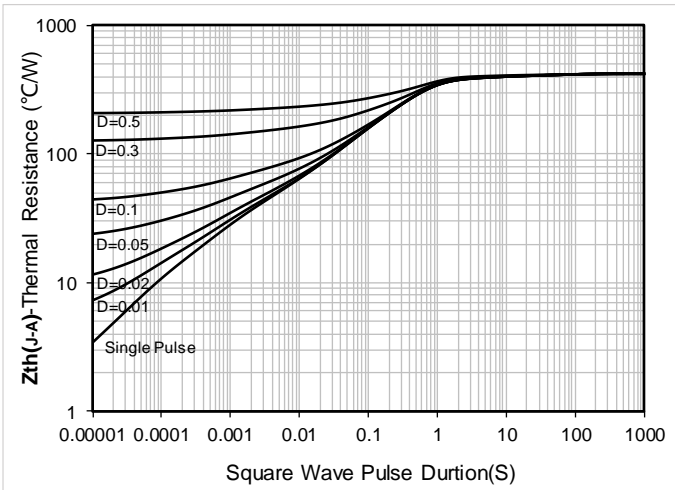


Figure 13. Maximum Transient Thermal Impedance

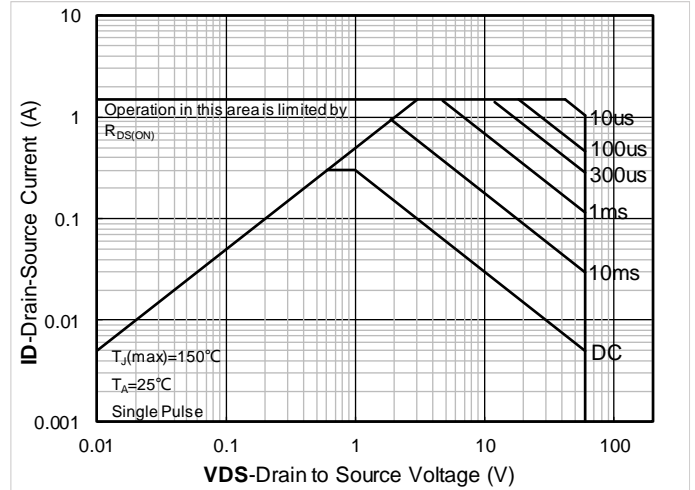


Figure 14. Safe Operation Area

## ■ Test Circuits & Waveforms

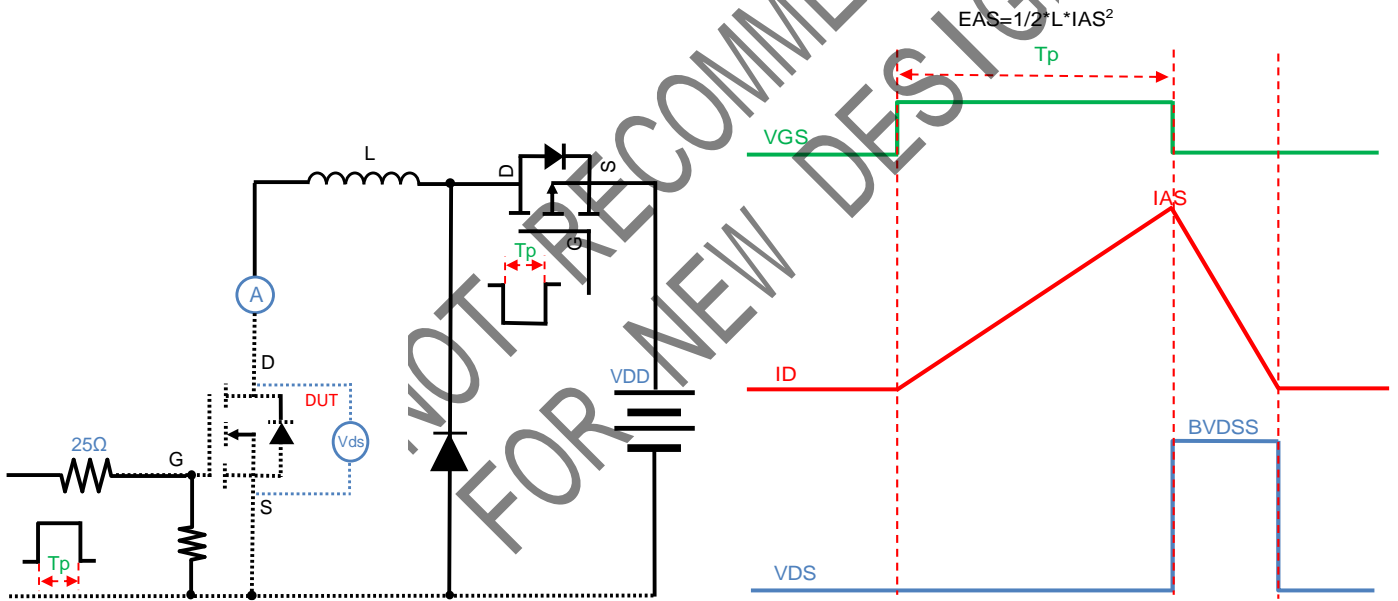


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

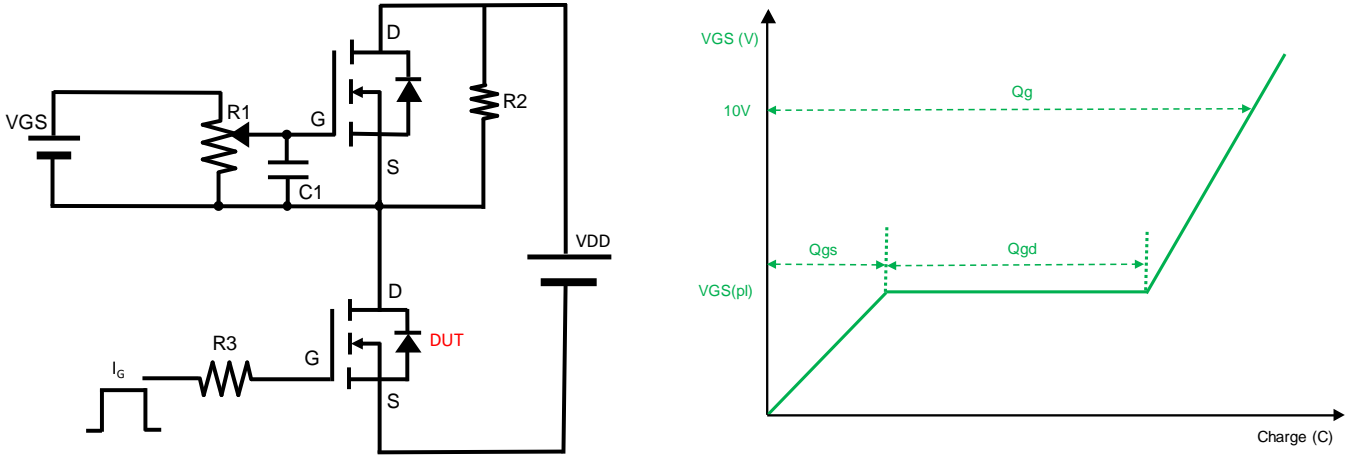


Figure B. Gate Charge Test Circuit & Waveform

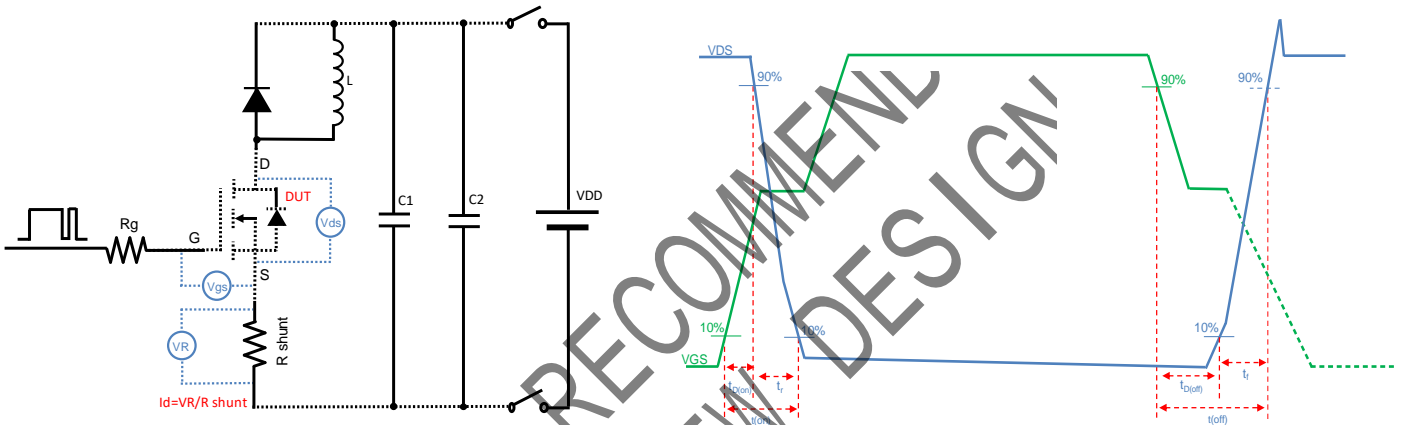


Figure C. Resistive Switching Test Circuit & Waveform

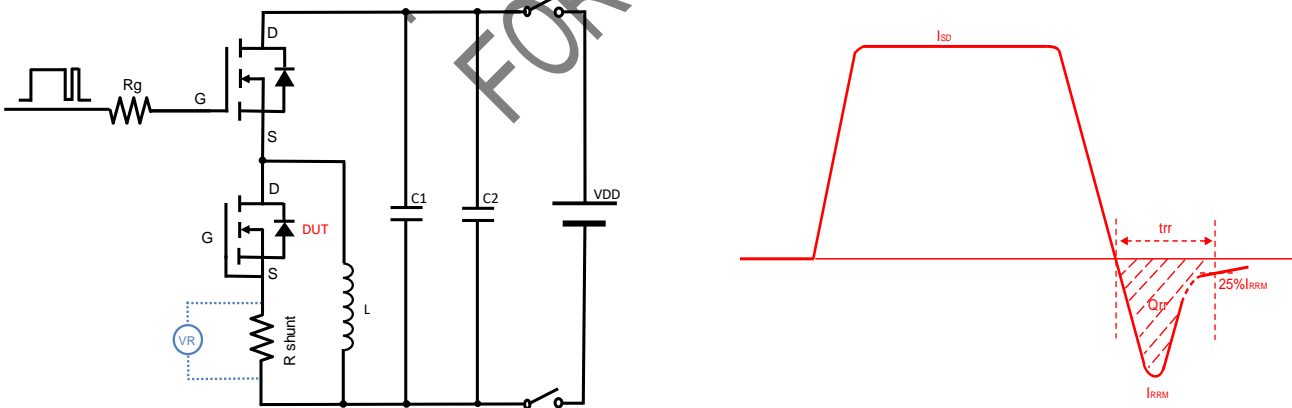
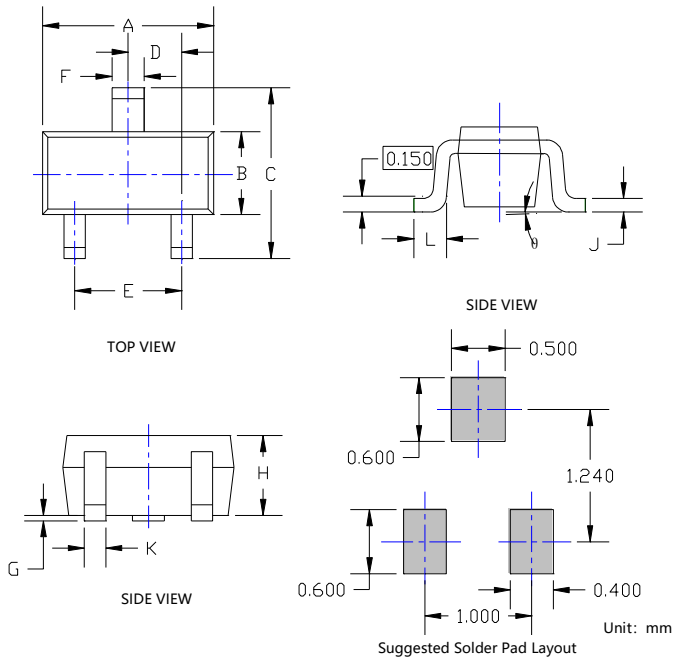


Figure D. Diode Recovery Test Circuit & Waveform

## ■ SOT-523 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.059	0.067	1.500	1.700
B	0.030	0.033	0.750	0.850
C	0.057	0.069	1.450	1.750
D	0.020TYP		0.500TYP	
E	0.035	0.043	0.900	1.100
F	0.010	0.018	0.250	0.450
G	0.000	0.004	0.000	0.100
H	0.024	0.031	0.600	0.800
J	0.004	0.008	0.100	0.200
K	0.006	0.014	0.150	0.350
L	0.010	0.018	0.260	0.460
θ	0°	8°	0°	8°

**NOTE:**  
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.  
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

NOT RECOMMENDED FOR NEW DESIGN



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